WHAT IS CLAIMED IS:

1. An apparatus comprising:

first and second bumps;

a first metal layer coupled to the first and second bumps, the first metal layer being formed in a trench of a dielectric layer, the first metal layer being coupled to a top metal layer of an integrated circuit die, the first metal layer being adapted to transfer current from the first and second bumps to the top metal layer of the integrated circuit die.

2. The apparatus of Claim 1, wherein the first and second bumps are Controlled Collapse Chip Connection bumps.

3. The apparatus of Claim 1, wherein the first and second bumps are coupled to first and second solder bumps of a substrate.

4. The apparatus of Claim 1, wherein the first metal layer is about 10 to 50 microns thick.

5. The apparatus of Claim 1, wherein the first metal layer comprises electroplated copper.

6. The apparatus of Claim 1, wherein the first metal layer is deposited in vias over a first base layer metallization, which is deposited over the top metal layer of the integrated circuit die.

7. The apparatus of Claim 1, further comprising a first dielectric layer enclosing the first metal layer.

8. The apparatus of Claim 7, wherein the first dielectric layer comprises a self-planarizing, photo-definable polymer.

9. The apparatus of Claim 7, wherein the first dielectric layer comprises a self-planarizing, non-photo-definable polymer.

10. The apparatus of Claim 1, further comprising a second metal layer over the first metal layer, the second metal layer being coupled to the first bump, a third bump and the first metal layer, the second metal layer being adapted to transfer current from the first and third bumps to the first metal layer, which is adapted to transfer current to the top metal layer of the integrated circuit die.

11. The apparatus of Claim 10, wherein the second metal layer is orthogonal to the first metal layer.

12. The apparatus of Claim 1, further comprising diffusion barriers over and on sides of the first metal layer.

13. A method comprising:

forming a first metal layer over a first base layer metallization, the first base layer metallization contacting a top metal layer of an integrated circuit die;

forming a first dielectric layer over the first metal layer;

forming vias in the first dielectric layer;

forming a second base layer metallization in the vias of the first dielectric layer; and

forming bumps over the second base layer metallization, the top metal layer being coupled to the first metal layer, the first metal layer being adapted to transfer current from the bumps to the top metal layer of the integrated circuit die.

14. The method of Claim 13, wherein the first and second bumps are Controlled Collapse Chip Connection bumps.

15. The method of Claim 13, wherein the first metal layer is about 10 to 50 microns thick.

16. The method of Claim 13, wherein said forming the first metal layer over the first base layer metallization comprises electroplating copper to the first base layer metallization.

17. The method of Claim 13, further comprising attaching the bumps to solder bumps of a substrate.

18. The method of Claim 13, further comprising forming the first base layer metallization in vias of a polyimide layer.

19. The method of Claim 13, further comprising forming the first base layer metallization in vias of a benzocyclobutene layer.

20. The method of Claim 13, further comprising forming the first base layer metallization in vias of an epoxy layer.

21. The method of Claim 13, wherein said forming a first dielectric layer uses a self-planarizing, photo-definable polymer.

22. The method of Claim 13, wherein said forming a first dielectric layer uses a self-planarizing, non-photo-definable polymer.

23. The method of Claim 13, further comprising forming a second metal layer after forming the first metal layer and before forming the bumps, the second metal layer being coupled to the at least two bumps and the first metal layer, the second metal layer adapted to transfer current from the at least two bumps to the first metal layer, which is adapted to transfer current to the top metal layer of the integrated circuit die.

24. The method of Claim 23, wherein the second metal layer is orthogonal to the first metal layer.

25. The method of Claim 13, further comprising forming diffusion barriers over and on sides of the first metal layer.

26. A method comprising:

forming a first metal layer over a first barrier seed layer, the first barrier seed layer contacting a top metal layer of an integrated circuit die;

forming a passivation layer over the first metal layer;

forming a polyimide layer over the passivation layer;

developing vias in the polyimide layer;

forming a seed barrier layer in the vias; and

forming first and second bumps over the seed barrier layer.

27. The method of Claim 26, wherein the first metal layer is 10-50 μm thick.

28. The method of Claim 26, further comprising:

forming a dielectric layer over a passivation layer over the top metal layer of the integrated circuit die;

developing vias in the dielectric layer; and

forming the first barrier seed layer in the vias and over the dielectric layer.